Amendment to Claims

1 (currently amended). An array of nonvolatile memory cells, each cell comprising a first conductive gate, two conductive floating gates, and two source/drain regions, the source/drain regions being regions of a first conductivity type in a semiconductor substrate;

wherein in each row of the array, all the first conductive gates are connected together;

wherein in each column of the array, for any two consecutive memory cells, one source/drain region of one of the cells and one source/drain region of the other one of the cells are provided by a contiguous region of the first conductivity type in the semiconductor substrate, each contiguous region providing source/drain regions to only two of the memory cells in said column of the memory cells;

wherein the array also comprises a plurality of bitlines overlying the semiconductor substrate, ~~the bitlines~~ each bitline being connected to the source/drain regions of a plurality of the memory cells of a column of the array.

2 (original). The array of Claim 1 wherein at least one bitline is connected to one source/drain region of each memory cell in two columns of the memory cells.

3 (original). The array of Claim 2 wherein in said two columns of the memory cells, the source/drain regions of one of the columns are separated from the source/drain regions of the other one of the columns by field isolation regions in the semiconductor substrate.

4 (original). The array of Claim 1 wherein in at least two columns of the memory cells, at least one contiguous region provides exactly two source/drain regions for one of the columns and exactly two source/drain regions in the other one of the columns.

5 (original). The array of Claim 1 wherein each memory cell has one of its source/drain regions connected to one of the bitlines, and the other one of its source/drain regions connected to another one of the bitlines.

6 (original). The array of Claim 1 wherein each memory cell also comprises two second conductive gates, and in each row one second conductive gate of each memory cell is connected to one second conductive gate of every other memory cell in that row.

7 (original). The array of Claim 6 wherein:

the first conductive gates in each row are provided by a first conductive line formed over the semiconductor substrate; and

for each row, the array has two second conductive lines over the semiconductor substrate, each of the second conductive lines providing one second conductive gate to each memory cell in the row.

8 (currently amended). A method for manufacturing an integrated circuit comprising an array of nonvolatile memory cells, the method comprising:

for each memory cell, forming a first conductive gate, two conductive floating gates, and two source/drain regions, the source/drain regions being regions of a first conductivity type in a semiconductor substrate;

wherein in each row of the array, all the first conductive gates are connected together;

wherein in each column of the array, for any two consecutive memory cells, one source/drain region of one of the cells and one source/drain region of the other one of the cells are provided by a contiguous region of the first conductivity type in the semiconductor substrate, each contiguous region providing source/drain regions to only two of the memory cells in said column of the memory cells;

wherein the method further comprises forming a plurality of bitlines over the semiconductor substrate, ~~the bitlines~~ each bitline being connected to the source/drain regions of a plurality of the memory cells of a column of the array.

9 (original). The method of Claim 8 wherein at least one bitline is connected to one source/drain region of each memory cell in two columns of the memory cells.

10 (original). The method of Claim 9 wherein in said two columns of the memory cells, the source/drain regions of one of the columns are separated from the source/drain regions of the other one of the columns by field isolation regions in the semiconductor substrate.

11 (original). The method of Claim 8 wherein in at least two columns of the memory cells, at least one contiguous region provides exactly two source/drain regions for one of the columns and exactly two source/drain regions in the other one of the columns.

12 (original). The method of Claim 8 wherein each memory cell has one of its source/drain regions connected to one of the bitlines, and the other one of its source/drain regions connected to another one of the bitlines.

13 (original). The method of Claim 8 wherein each memory cell also comprises two second conductive gates, and in each row one second conductive gate of each memory cell is connected to one second conductive gate of every other memory cell in that row.

14 (original). The method of Claim 13 wherein:

the first conductive gates in each row are provided by a first conductive line formed over the semiconductor substrate; and

for each row, the array has two second conductive lines over the semiconductor substrate, each of the second conductive lines providing one second conductive gate to each memory cell in the row.

15 (new). The array of Claim 1 wherein:

each memory cell comprises an active area in the semiconductor substrate, the active area comprising two source/drain regions of the memory cell and a channel region of the memory cell, the channel region extending between the two source/drain regions; and

the array further comprises one or more field isolation regions which are dielectric regions extending below a top surface of the semiconductor substrate, each field isolation

region extending through the array between the active areas of the memory cells of one of the columns and the active areas of the memory cells of another one of the columns.

16 (new). The array of Claim 15 wherein the active areas of the memory cells of each column are part of a contiguous active area of the semiconductor substrate.

17 (new). The array of Claim 1 wherein each memory cell comprises a channel region extending between two source/drain regions of the memory cell in a column direction, the channel region being a region the semiconductor substrate.

18 (new). The array of Claim 17 wherein in each memory cell, the first conductive gate controls a conductivity of a portion of the channel region, and the floating gates are positioned laterally on opposite sides of the first conductive gate.

19 (new). The method of Claim 8 wherein:

each memory cell comprises an active area in the semiconductor substrate, the active area comprising two source/drain regions of the memory cell and a channel region of the memory cell, the channel region extending between the two source/drain regions; and

the method further comprises forming one or more field isolation regions which are dielectric regions extending below a top surface of the semiconductor substrate, each field isolation region extending through the array between the active areas of the memory cells of one of the columns and the active areas of the memory cells of another one of the columns.

20 (new). The method of Claim 19 wherein the active areas of the memory cells of each column are part of a contiguous active area of the semiconductor substrate.

21 (new). The method of Claim 8 wherein each memory cell comprises a channel region extending between two source/drain regions of the memory cell in a column direction, the channel region being a region the semiconductor substrate.

22 (new). The method of Claim 21 wherein in each memory cell, the first conductive gate controls a conductivity of a portion of the channel region, and the floating gates are positioned laterally on opposite sides of the first conductive gate.

23 (new). An array of nonvolatile memory cells, each cell comprising a first conductive gate, two conductive floating gates, and two source/drain regions, the source/drain regions being regions of a first conductivity type in a semiconductor substrate;

wherein in each row of the array, all the first conductive gates are connected together;

wherein the array also comprises a plurality of bitlines overlying the semiconductor substrate, each bitline being connected to the source/drain regions of a plurality of the memory cells of a column of the array;

wherein each memory cell comprises an active area in the semiconductor substrate, the active area comprising two source/drain regions of the memory cell and a channel region of the memory cell, the channel region extending between the two source/drain regions; and

wherein the array further comprises one or more field isolation regions which are dielectric regions extending below a top surface of the semiconductor substrate, each field isolation region extending through the array between the active areas of the memory cells of one of the columns and the active areas of the memory cells of another one of the columns.

24 (new). The array of Claim 23 wherein the active areas of the memory cells of each column are part of a contiguous active area of the semiconductor substrate.

25 (new). The array of Claim 23 wherein each memory cell comprises a channel region extending between two source/drain regions of the memory cell in a column direction, the channel region being a region the semiconductor substrate.

26 (new). The array of Claim 23 wherein in each memory cell, the first conductive gate controls a conductivity of a portion of the channel region, and the floating gates are positioned laterally on opposite sides of the first conductive gate.

27 (new). A method for manufacturing an integrated circuit comprising an array of nonvolatile memory cells, the method comprising:

for each memory cell, forming a first conductive gate, two conductive floating gates, and two source/drain regions, the source/drain regions being regions of a first conductivity type in a semiconductor substrate;

wherein in each row of the array, all the first conductive gates are connected together;

wherein the method further comprises forming a plurality of bitlines over the semiconductor substrate, each bitline being connected to the source/drain regions of a plurality of the memory cells of a column of the array.

wherein each memory cell comprises an active area in the semiconductor substrate, the active area comprising two source/drain regions of the memory cell and a channel region of the memory cell, the channel region extending between the two source/drain regions; and

wherein the method further comprises forming one or more field isolation regions which are dielectric regions extending below a top surface of the semiconductor substrate, each field isolation region extending through the array between the active areas of the memory cells of one of the columns and the active areas of the memory cells of another one of the columns.

28 (new). The method of Claim 27 wherein the active areas of the memory cells of each column are part of a contiguous active area of the semiconductor substrate.

29 (new). The method of Claim 27 wherein each memory cell comprises a channel region extending between two source/drain regions of the memory cell in a column direction, the channel region being a region the semiconductor substrate.

30 (new). The method of Claim 27 wherein in each memory cell, the first conductive gate controls a conductivity of a portion of the channel region, and the floating gates are positioned laterally on opposite sides of the first conductive gate.